design ideas

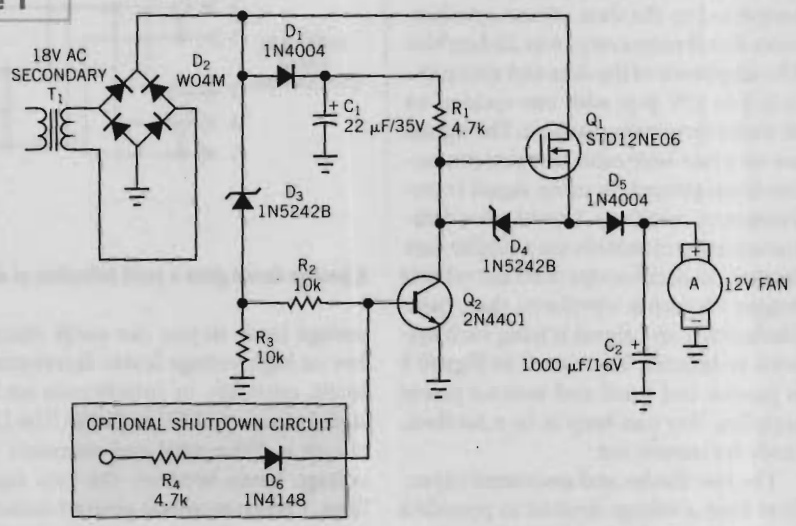
Edited by Bill Travis and Anne Watson Swager

MOSFET switch provides efficient ac/dc conversion

Spehro Pephany, Trexon Inc, Toronto, ON, Canada

OCCASIONALLY, YOU HAVE access to a transformer for powering a dc circuit, but its output voltage is much higher than that required for the dc voltage. The full-wave-rectified and filtered output of an ac input voltage V_X, is $V_{DC} = 1.414V_X - 2V_F$, where V_F is the forward drop in the rectifier (approximately 0.7V). For example, if you require 12V dc to power a small cooling fan drawing 100 mA and the ac voltage is 18V, a full-wave rectifier and filter results in a 24V-dc output. Although you can regulate the voltage down to 12V dc by using a simple three-terminal regulator (such a μA7812), the result is wasted power of approximately 1.3W. This waste means that you must provide for heat removal, somewhat defeating the purpose of including the cooling fan. If you use a typical 100 × 100-mm, 12V-dc fan rated at 0.45A, the typical heat loss is approximately 2.5W, increasing to 5W at full load. In many applications, this level of loss is unacceptable, so you'd have to use an extra transformer secondary, a dc/dc converter, or a switching regulator. The circuit in **Figure 1** uses a MOSFET switch and diode to effectively draw current from the transformer when the voltage is close to the desired level of 12V dc.

Figure 1



Using a MOSFET circuit, you can efficiently convert the too-high voltage of a leftover transformer to a lower dc level.

The full-wave bridge, D_2, rectifies the 18V-ac signal. The diode, D_1, and C_1 provide a gate bias voltage of approximately 24V dc. This voltage drives the gate of Q_1 through R_1, shunted by D_4, which maintains the gate voltage at a maximum of 12V relative to the source, even during transient conditions. As the bridge-rectifier output increases from 0V to the peak of approximately 24V each half-cycle, the bias voltage holds the MOSFET on until the input voltage reaches the breakdown voltage of D_3 (12V) plus the $V_{BE(ON)}$ of Q_2, or approximately 12.7V. At that point, Q_2 turns on, turning Q_1 off. The output filter capacitor, C_2, charges through D_5. As the rectifier output voltage decreases from 24 to 0V, Q_2 again turns off at approximately 12.7V, allowing Q_1 to turn on and provide another pulse of current to charge C_2. C_2 provides power for the load between the pulses, which occur at 240 Hz with a 60-Hz input. Thus, power drain from the transformer occurs in short pulses, much in the manner of a typical bridge-rectifier/output-filter arrangement but at double the frequency. If you want to turn the fan off with a logic signal, you can add R_4 and D_6. When you apply a logic-high signal to the input, Q_2 conducts, turning the MOSFET off. (DI #2484)

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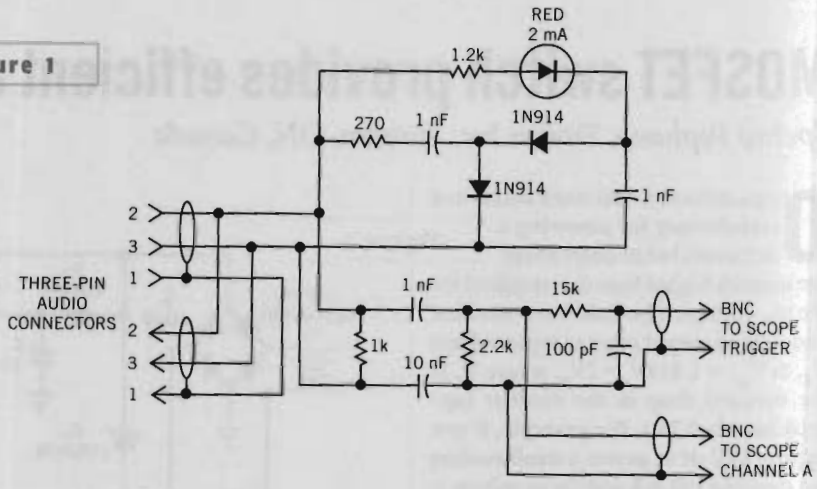
Passive circuit monitors AES data

Wayne Sward, Bountiful, UT

THE CIRCUIT IN **Figure 1** efficiently monitors common digital-audio signals. One format for such signals is the Audio Engineering Society (AES) 44.1- or 48-kHz standard. Typically, the data consists of a serial data stream with a data rate of approximately 1 Mbps. A lower frequency pulse interspersed in the data stream synchronizes data frames every 16 to 20 data bits. The amplitude of the data and sync pulses is 3 to 12V p-p, with one cycle of an ac wave representing each bit. The signals are on a two-wire cable that you can isolate from ground by using signal transformers or capacitors. Several other data-transmission standards use a similar data format. An oscilloscope does not reliably trigger on such a waveform; thus, troubleshooting and signal tracing such systems is difficult. The circuit in **Figure 1** is passive and small and uses no power supplies. You can keep it in a toolbox, ready for instant use.

Figure 1



A passive circuit gives a good indication of data activity on digital-audio lines.

The two diodes and associated capacitors form a voltage doubler to provide a bias voltage of approximately −2 to −10V. The 2-mA LED connects between one of the signal lines and this bias voltage. Whenever the signal-line voltage exceeds approximately 1.5V, the LED turns on. At a data rate of nearly 1 MHz, the LED appears to continuously glow when good data is present. The LED's intensity is proportional to the peak-to-peak voltage level, so you can easily observe low or high voltage levels. Intermittent levels, crosstalk, or interference on the signal causes the LED to flicker. The LED circuit is differential and measures the voltage levels between the two signal lines. Common-mode ground noise or hum do not affect the LED's display. The voltage doubler is an efficient way to increase the sensitivity of the LED without an additional power supply.

The two coupling capacitors sample the high-frequency data waveform but reject any low-frequency common-mode noise or hum. You can display the data waveform on an oscilloscope to more closely inspect the wave shape. The 15-kΩ resistor and 100-pF capacitor form a simple but effective filter to detect the sync bit in the data stream. You feed this sync bit to the external sync input of the oscilloscope, resulting in a stable display of the data frame. The coupling capacitors avoid creating a ground loop between the signal lines and the grounded, shielded input of the oscilloscope. You can readily monitor data amplitude, waveshape, and activity of individual bits with the oscilloscope. (DI #2482)

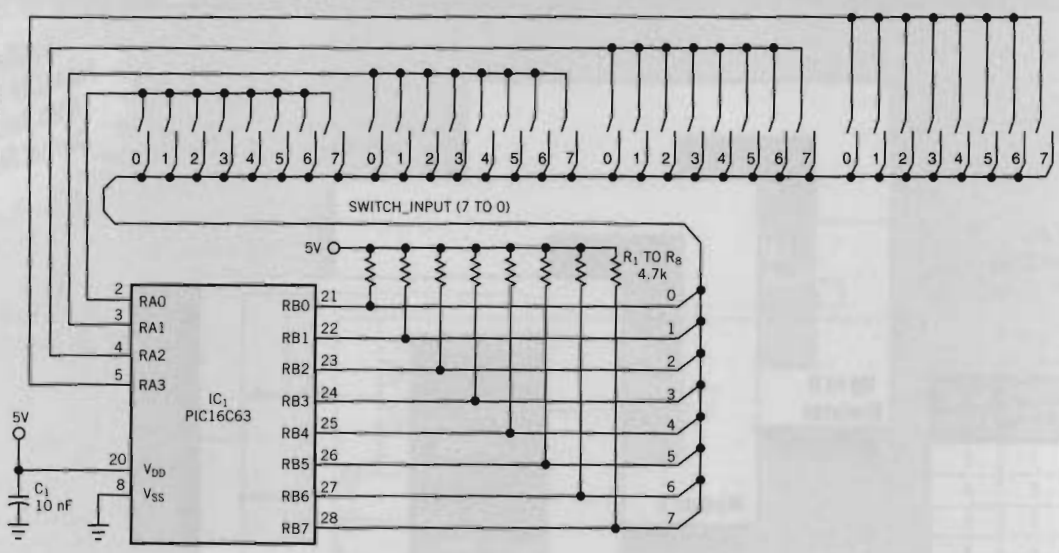
TO VOTE FOR THIS DESIGN, CIRCLE NO. 312

µC multiplexes DIP switches to I/O port

Gregory Willson, ACS Defense Inc, Warrenton, VA

AT TIMES, A µC must read a large number of DIP switches, such as for system identification, bus-address setup, manual configuration, or other purposes. However, the available number of I/O lines is sometimes not enough to assign a switch to each one. You can use multiplexer ICs to share one I/O port with multiple switches, but they complicate the circuit, dissipate additional power, and consume precious board real estate. **Figure 1** shows a method of multiplexing 32 DIP switches using only 12 I/O pins and eight pullup resistors. Four 8-bit DIP switches connect in parallel to a single 8-bit I/O port. A pullup resistor on each port pin defaults the input to a high state; a switch closure pulls the input to

Figure 1



Using only 12 I/O pins, a μC can read 32 DIP switches.

a low state. The key to multiplexing the DIP switches is to ground each set of eight switches in turn using output pins from a second I/O port.

To deselect a set of switches, the controlling-port pin acts as an input, rendering it a high-impedance port. In this way, 12 I/O pins can read 32 switches, and 16 I/O pins can read 64 switches. Select the values of the pullup resistors to limit the total current into the controlling-port pin to less than the maximum sink current. Some μCs, such as the Microchip PIC16C6x family, provide the ability to enable weak internal pullups on I/O port pins. By using this feature, you can eliminate the eight external pullup resistors. The code fragment in **Listing 1** illustrates reading the four 8-bit DIP switches and storing the results, using a Microchip PIC16C63 μC. You can download **Listing 1** from *EDN*'s Web site, www.ednmag.com. Click on "Search Databases" and then enter the Software Design Center to download the file for Design Idea #2483. (DI #2483)

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LISTING 1—MULTIPLEXING DIP SWITCHES TO SINGLE I/O PORT

```
;Microcontroller Multiplexes Multiple DIP Switches to Single I/O Port
;Author: Gregg Willson, ACS Defense, Inc.

;Define constants
      list  p=16c63
#include    "c:\mpasm\P16C63.inc"

;Define RAM storage locations for DIP switch values
TMP0  equ   h'20'
TMP1  equ   h'21'
TMP2  equ   h'22'
TMP3  equ   h'23'

;Main Routine
Read_32_DIP_Switches
      call  Initialize_Ports  ;Setup ports for multiplexing
      movlw b'11111110' ;Get ready to make port A, bit 0 an output
      call  Read_DIP_Sw ;Read the first DIP switch
      movwf TMP0        ;Save in temporary register
      movlw b'11111101' ;Get ready to make port A, bit 1 an output
      call  Read_DIP_Sw ;Read the second DIP switch
      movwf TMP1        ;Save it
      movlw b'11111011' ;Get ready to make port A, bit 2 an output
      call  Read_DIP_Sw ;Read the third DIP switch
      movwf TMP2        ;Save it
      movlw b'11110111' ;Get ready to make port A, bit 3 an output
      call  Read_DIP_Sw ;Read the fourth DIP switch
      movwf TMP3        ;Save it
      return
; DONE

;Subroutines
Initialize_Ports
      bcf   STATUS, RP0 ;Select register Bank 0
      movlw b'00000000' ;Default port A outputs to 0 to ground switches
      movwf PORTA
      bsf   STATUS, RP0 ;Select register Bank 1
      movlw b'11111111' ;Make port B all inputs
      movwf TRISB
      movwf TRISA       ;Make port A all inputs initially
      bcf   OPTION_REG, 7     ;Option: Enable weak internal pullups on port B
      return

Read_DIP_Sw
;Enable DIP Switch based on W register value
      bsf   STATUS, RP0 ;Select register Bank 1
      movwf TRISA       ;DIP switch is now selected
;Read the data
      bcf   STATUS, RP0 ;Select register Bank 0
      movf  PORTB, W    ;Put switch values in W register
      return

      END
```

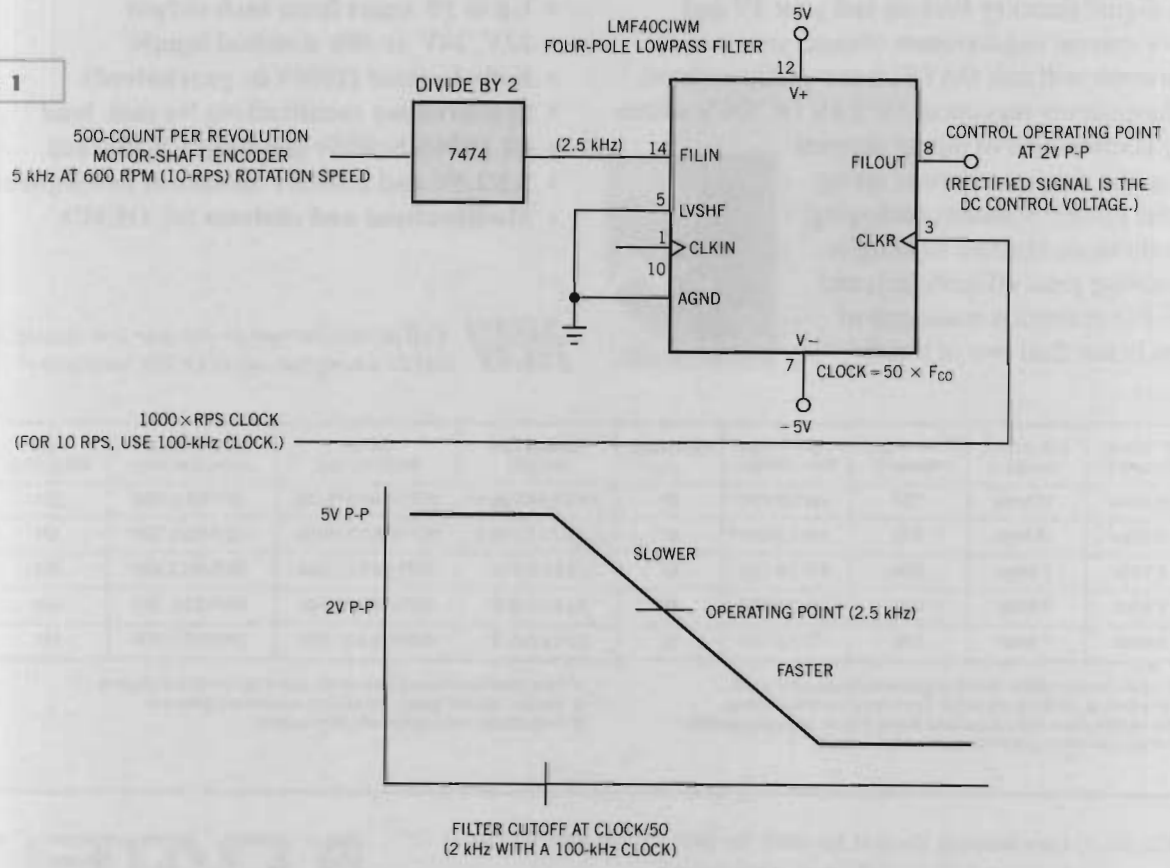
Switched-capacitor IC controls feedback loop

Dave Sargent, IBM Research, San Jose, CA

You can implement a simple control loop with a constant setpoint over a wide range of control by using a switched-capacitor filter. The circuit controls motor speed over 1 to 200 Hz or 60 to 12,000 rpm. In **Figure 1**, a National LMF40CIWM four-pole lowpass filter is the heart of the design. This filter has a cutoff frequency defined by the clock divided by 50. Consider this filter as a difference amplifier that compares the difference between two frequencies. The relationship between the clock divided by 50 and the 500-count encoder divided by 2 is such that when the clock rate is 1000 times the revolutions per second of the motor, the signal frequency from the encoder is at approximately the midpoint of the filter response. This midpoint is the point of zero error and is approximately 2V p-p. The rectified output serves as the dc setpoint voltage for the control loop. If the motor speed increases, the voltage decreases, and if the motor slows down, the voltage increases. As simple as the method is, it can drive a motor-control chip and provide good speed regulation.

You can use the method to control other servo loops that provide a feedback frequency within the range of the filter. The big advantage of this scheme is that the setpoint remains constant with a range of speed settings. Another advantage is that the clock provides direct speed calibration thanks to the 1000-to-1 relationship between the clock and the rotational speed of the motor. **Figure 2** shows some circuit details for enhanced operation. To cover the higher speed range, you need an additional divide by 10 to stay within the frequency range of the filter. An example is given for 6- and 60-Hz rotational speeds. Conventional op-amp circuits buffer and rectify the output of the filter. The application uses one of many full-wave op-amp-rectifier circuits that follow a buffer with a gain of 2. After rectification, the 75-kΩ resistors and 0.1-μF capacitor provide some filtering and time-constant conditioning. You set the gain of op amp 1 so its output dc voltage is 2.5V at the operating point. Op amp 2 offsets this voltage and moves the operating point to 0V when no speed error is present. The offset-adjust trimmer allows for minor variations and calibrates the actual rotational speed to the clock signal. Op

Figure 1

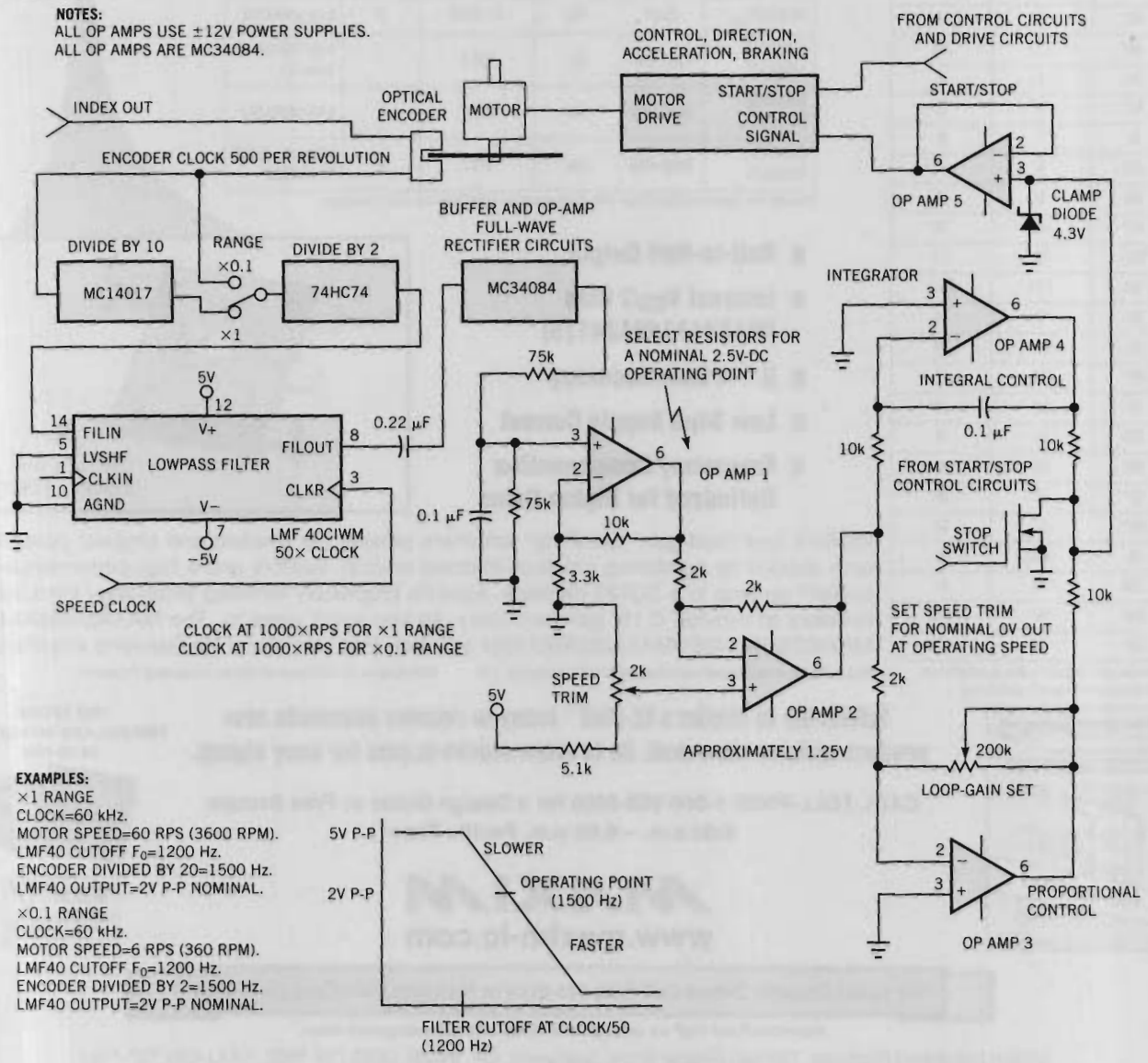


A lowpass filter is the heart of a wide-range control loop.

amp 3 provides gain for the proportional signal.

You can use a fixed resistor in place of the 200-kΩ trimmer. Op amp 4 is an integrator circuit that provides the classical integral control for the loop. The integrator makes up for errors in the following control circuits and motor characteristics throughout the control range. The integrator control-point output voltage therefore changes at different speed settings. Buffer op amp 5 sums the proportional and integral signals at its input. A clamp diode limits the positive drive voltage and prevents any negative excursions from driving the loop to a latch-up condition. In an application, the clamping limits the output to 4.3A, because the motor-control circuit has a drive characteristic of 1A per volt. When the motor stops, the FET stop switch clamps the control signal to zero. Additional circuits control acceleration rate, braking rate, and direction. The speed accuracy for the system is a nominal 0.002% throughout the range. The speed clock comes from a DDS chip, and all the above functions are under control of a PC or front-panel switch settings. (DI #2486)

Figure 2



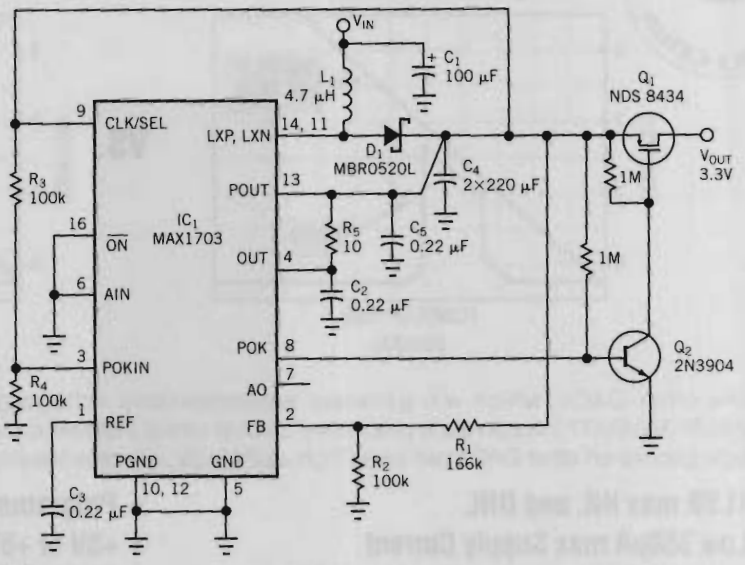
A wide-range control circuit uses two ranges for maximum resolution.

Simple circuit disconnects load

Larry Suppan, Maxim Integrated Products, Sunnyvale, CA

Placing a load-disconnect circuit on the output of a boot-strapped step-up regulator allows the regulator to start with load currents much higher than would otherwise be possible (**Figure 1**). During shutdown, the disconnect completely isolates the battery from the load. The circuit boosts a single NiMH-cell output to 3.3V and delivers output currents to 600 mA. Step-up regulators are excellent for portable applications because they exhibit high efficiency, low supply current (120 μA operating, 20 μA in shutdown), and ample current once started. Many, however, cannot start with maximum load from low supply voltages, such as those from single-cell batteries. This problem arises because most low-voltage CMOS boost regulators derive power from their own outputs, which equal V_{IN} minus a diode drop at start-up. Low values of input voltage don't allow the switching transistor to become fully enhanced at start-up, so the transistor presents a high impedance that limits the peak inductor current. As a result, the circuit cannot produce enough current to simultaneously supply the load and charge the output capacitor.

Figure 1

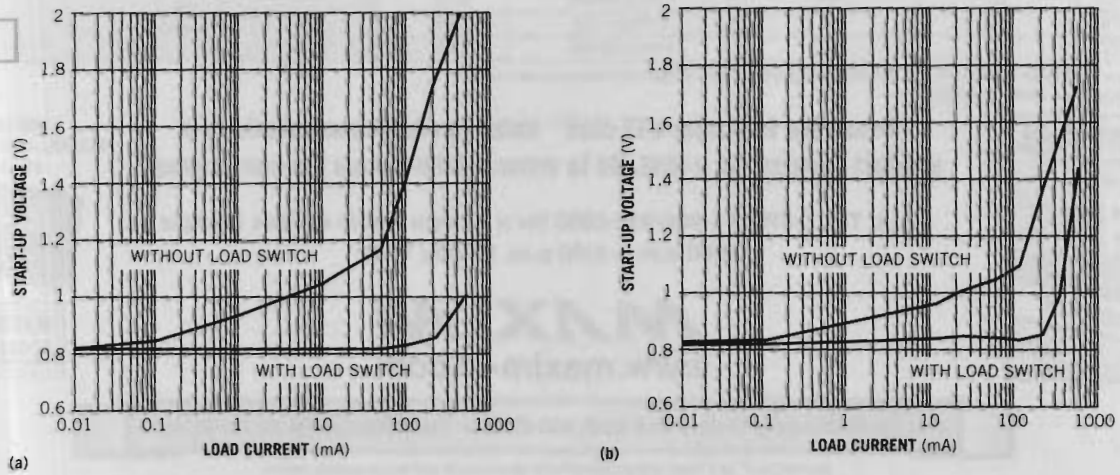


NOTE:
HEAVY LINES INDICATE HIGH-CURRENT PATHS.

The addition of a couple of transistors enables a switching regulator to start with full load and low input voltages.

To get around this problem and ensure reliable start-ups, most regulator ICs incorporate an undervoltage lockout (UVLO). IC_1, for example, is a synchro-

Figure 2



The load-disconnect switch in Figure 1 allows the regulator to start up with heavy loads and low input voltages (a). A slight modification of the circuit in Figure 1 provides 5V-output operation (b).

nous boost converter whose bootstrapped operation cannot start until its output voltage exceeds the internal UVLO threshold of 2.3V. You can overcome this start-up limitation with an external power MOSFET, Q_1, operating as a load-disconnect switch, and by using the power-OK (POK) comparator built into many low-voltage switching regulators. R_3 and R_4 set the POK threshold at 2.5V, allowing V_{IN} to rise above the UVLO threshold. Q_2 inverts the POK output before driving Q_1. Q_1 disconnects the load, allowing V_{OUT} to rise to a level (above UVLO) that ensures full enhancement of Q_1 when it turns on. As a result, the circuit can start under full load with input voltages as low as 0.8V (**Figure 2a**). Because the circuit takes the regulator feedback before this switch, the MOSFET you choose for a given application depends on the load current and minimum acceptable level of load regulation. The MOSFET shown is a low-threshold device. Connecting the FB terminal (Pin 2) to ground and removing R_1 and R_2 produces a 5V regulated output, whose performance is similar to that of the 3.3V version (**Figure 2b**). (DI #2487)

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Follow the debouncing flip-flops

Ray Scott and John Stanley, Airport Systems International, Overland Park, KS

During a recent development effort, we could not find literature detailing how to debounce an spst momentary switch using only logic (no capacitors, Schmitt triggers, or other components). Our application placed the spst switches several feet from the logic board, and both noisy switches and line transients caused false triggers. Many methods simulate a debounce by checking the state of the switch on clock edges and summing the checks over time, but our application required no transitions during the qualification time before acknowledgment of a key press. Thus, the switches can work effectively in noisy environments over reasonably long distances. **Figure 1** illustrates a means of debouncing a momentary switch for both the make and the break operations. Designers often use programmable logic to debounce momentary switches used in keypads, in keyboards, or as configuration inputs. Flip-flops are usually precious commodities in programmable logic, whereas logic gates are available in greater abundance. The design in **Figure 1** minimizes the use of flip-flops.

The circuitry monitors the state of the Switch input. Once the circuit detects a transition, a "qualifying" time of two Debounce_Clock periods begins. If at any time during the qualifying time the Switch input returns to its original state, indicating switch bounce or an electrical transient, the circuitry returns to its starting state and begins looking for another transition. The Switch input must be completely stable for two positive transitions of the Debounce_Clock input before the Switch_Debounced output will change. A frequency of approximately 15 Hz (or a period of 66 msec) for the Debounce_Clock input works well, even for low-cost, "noisy" switches. You can delete the reset logic if you are unconcerned with the power-on state of the Switch_Debounced output. Following power-on, the output will be correct after two clock periods. (DI #2481)

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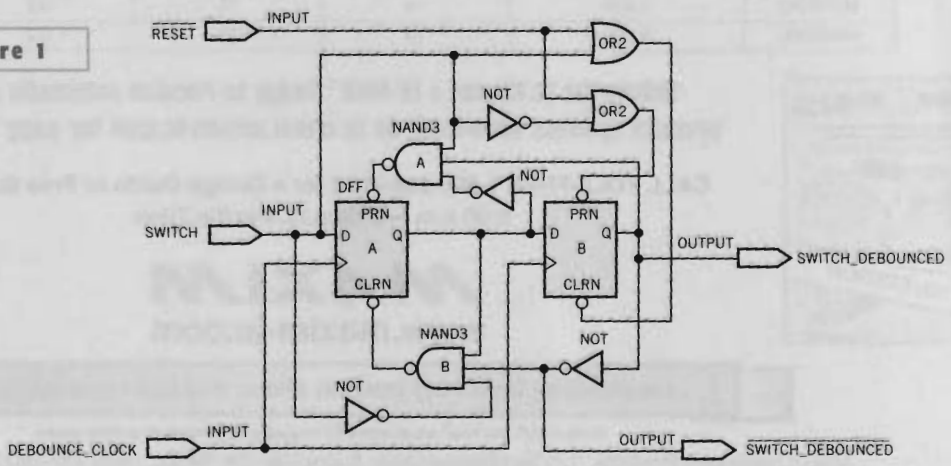
Figure 1



A debouncing circuit using programmable logic makes frugal use of flip-flops.

Inductorless converter provides high efficiency

Sam Nork, Linear Technology Corp, Milpitas, CA

TWO COMMON METHODS exist for generating a regulated dc output voltage that is lower than the input voltage. The first approach is to use a low-dropout (LDO) regulator. LDO regulators are small, easy to use, and inexpensive, but all the output current must also flow through the input; hence, they exhibit low efficiency. The second approach is to use an inductor-based switching regulator. Inductor-based switchers can be efficient, but they tend to be more complex, costly, and area-consuming than their LDO-regulator counterparts. A third option retains the simplicity and size of an LDO regulator but enjoys the high efficiency usually reserved for inductor-based circuits. The circuit in **Figure 1** uses switched-capacitor techniques to achieve high-efficiency step-down conversion without an inductor.

The circuit produces a regulated 2V output with as much as 100 mA of load-current capability. IC_1, an LTC1503-2, has an input range of 2.4 to 6V, allowing the IC to take power from either a single Li-ion cell or a three-cell NiMH battery. IC_1 uses fractional-conversion techniques to achieve efficiencies typically more than 25% higher than that of an LDO regulator (**Figure 2**). Internal control circuitry ensures that the device operates with the optimal step-down ratio as the input voltage and load conditions vary. You need only four small ceramic capacitors to make a complete step-down supply. Quiescent current of 25 µA typical and the small MSOP-8 package make the circuit ideal for handheld devices. (DI #2485)

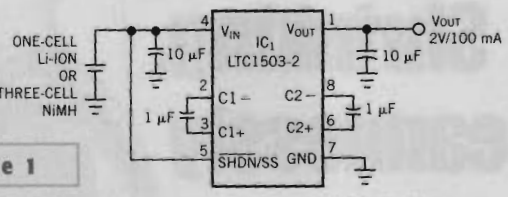


Figure 1

Eschew bulky inductors, using switched-capacitor step-down conversion.

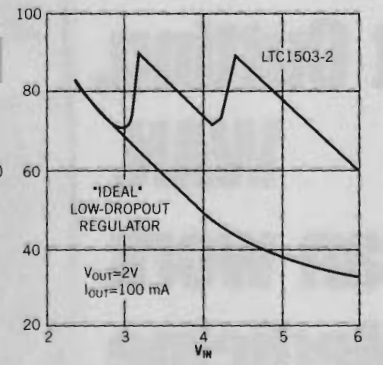


Figure 2

Switched-capacitor conversion yields higher efficiency than LDO regulators.

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